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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/681,994	07/05/2001	Louis R. Nerone	GEC 2 0585	5848

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EXAMINER
LEE, WILSON

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/681,994	NERONE, LOUIS R.	
	Examiner	Art Unit	
	Wilson Lee	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,4,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

IDS

The reference Sullivan et al. (5,001,386) cited in the IDS faxed on 6/24/02 is cross through because it has already been considered in the IDS previously filed on 2/1/02.

Claim Rejections – 35 U.S.C. 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 4, 7, 8, 11 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Parker et al. (6,121,732).

Regarding Claim 1, Parker discloses a ballast circuit powered by an AC-to-DC converter (94) in operative connection with an input power source (92), the AC-to-DC converter (94) being configured to produce DC voltage, the ballast circuit comprising: a DC bus (e.g. the output of the smoothing circuit 96) in operative connection with the AC-to-DC converter (94), configured to receive the DC voltage; an inverter circuit (54)

configured in operative connection with the DC bus, configured to generate an asymmetric alternating current on a lamp input line (e.g. wires connected to the electrodes of the lamp) (See Abstract and Figures 4 and 5); and a gas discharge lamp (64) in operative connection to the lamp input line to receive the asymmetric alternative current.

Regarding Claim 4, Parker discloses that the inverter circuit includes a switching network including MOSFET transistor switches (66, 68) wherein the MOSFETs are configured to have unequal ON times (See Figures 7A and 7B).

Regarding Claim 7, Parker discloses a DC blocking capacitor (62) from the asymmetric alternating current (See Figure 5 and Col. 4, lines 23-24).

Regarding Claim 8, Parker discloses a method of supplying asymmetric alternating current to a gas discharge lamp (64) from a ballast, the method comprising: converting an AC voltage from an input power source (92) to produce a DC voltage on a DC bus line (e.g. the output of the smoothing circuit 96); inverting the DC voltage to produce an asymmetric alternating current on a lamp input (See Abstract and Figure 4); and supplying a gas discharge lamp (64) with the asymmetric alternating current in operative connection with the lamp input line (e.g. wires connected to the electrodes of the lamp) (See Figure 5).

Regarding Claim 11, Parker discloses that the inverting is performed by a switching network including MOSFET transistor switches (66, 68) wherein the MOSFETs are configured to have unequal ON times (See Figures 7A and 7B).

Regarding Claim 14, Parker discloses the method further including providing a DC blocking capacitor (62) configured to block DC current from the asymmetric alternating current (See Figure 5 and Col. 4, lines 23-24).

Regarding Claim 15, Parker discloses a ballast circuit powered by an AC-to-DC converter (94) in operative connection with an input power source (92), the AC-to-DC converter (94) being configured to produce DC voltage, the ballast circuit comprising: a DC bus (e.g. the output of the smoothing circuit 96) in operative connection with the AC-to-DC converter (94), configured to receive the DC voltage; a lamp input current generating circuit (54) configured in operative connection with the DC bus, configured to generate an asymmetric alternating current on a lamp input line (e.g. wires connected to the electrodes of the lamp) (See Abstract and Figures 4 and 5); and a gas discharge lamp (64) in operative connection to the lamp input line to receive the asymmetric alternative current.

Regarding Claim 16, Parker discloses a DC blocking capacitor (62) from the asymmetric alternating current (See Figure 5 and Col. 4, lines 23-24).

Claim Rejections – 35 U.S.C. 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker et al. (6,121,732) in view of Sullivan et al. (5,001,386).

Regarding Claims 2 and 9, as discussed above, Parker essentially discloses the claimed invention but fails to explicitly disclose the switching network including bipolar junction transistors. However, it is well known to any skilled in the art that any type of semiconductive switching means such as MOSFETs and bipolar transistors being used in the inverter of a lighting circuit would not change the scope of the inverter (See cited arts: Nakagawa and Grubbs). Such understanding is also disclosed in Sullivan cited by applicant is IDS filed on 2/1/02 that shows that any type of switches can be used in an inverter of a lighting circuit based on preference of the switching speed of the switches (e.g. MOSFETs have faster switching ability than bipolar transistors (See Col. 5, lines 29-41). It would have been obvious to one of ordinary skill in the art to use bipolar transistors in place of MOSFETs in Parker to render slower switching speed in order to attain a particular waveform at preferred frequency.

Regarding Claims 3 and 10, as discussed above, Parker essentially discloses the claimed invention but fails to disclose the beta values of the transistors are unequal. However, the beta values are totally affected by the collector current or the base current supplied to the transistors (See cited encyclopedia). It would have been obvious to one ordinary skill in the art to supply a desired base current input to a transistor (thereby rendering different beta value) in order to attain a preferred current output to the lamp, since it is held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Claims 5, 6, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker et al. (6,121,732) in view of Miyazaki et al. (5,057,721).

Regarding Claims 5 and 12, as discussed above, Parker essentially discloses the claimed invention but fails to disclose a back-to-back, series zener diodes bridging the gate and the source terminals of the MOSFETs. However, Miyazaki discloses a back-to-back, series zener diodes bridging the gate and the source terminals of the MOSFETs of an inverter circuit in order to protect the MOSFET from overvoltage (See Figure 1 and Col. 2, lines 52-60). It would have been obvious to one of ordinary skill in the art to provide a back-to-back, series zener diodes to bridge the gate and the source terminals of the MOSFETs of the inverter circuit in Parker in order to protect the MOSFET from overvoltage as taught by Miyazaki.

Regarding Claims 6 and 13, as discussed above, Parker essentially discloses the claimed invention but fails to disclose that the zener diodes have unequal voltage from each other. However, said (breakdown) voltage totally in fact depends on how a diode is manufactured (See cited encyclopedia). It would have been obvious to one of ordinary skill in the art to provide different zener diodes having different (breakdown) voltage in accordance with the transistor switches in order to obtain suitable overvoltage-limit protection on the switches. In addition, it is held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakagawa et al. (5,880,562) discloses that any switching means having a control terminal such as bipolar transistors, FETs, etc. can be used in the inverter of the lighting circuit (See Col. 8, lines 26-36).

Grubbs (4,723,098) discloses that any semiconductor switches can be used in the inverter and specifies that MOSFET has higher frequency response (Col. 5, lines 21-29).

Lesea (4,415,839) discloses that back-to-back zener diodes are used for providing clamping so as to prevent gate-source breakdown in transistor of the inverter (See Col. 11, lines 20-25).

Encyclopedia of Electronics written by Stan Gibilisco.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Wilson Lee whose telephone number is (703) 306-3426.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be

considered an official response must be clearly marked "DRAFT". The Technology Center Fax number is (703) 308-7722 or (703) 308-7724.

Patent Examiner

WL

9/6/02